Provisional Patent Application of

JINFENG ZU

For

TITLE: MANUFACTURING PROCESS FOR HIGH SPEED, ULTRA-BROADBAND AND LOW COST INTEGRATED OPTICAL MODULATOR BASED ON GRAPHENE

CROSS-REFERENCE TO RELATED APPLICATIONS: None.

FEDERALLY SPONSORED RESEARCH: None.

SEQUENCE LISTING: None.

SPECIFICATION

TECHNICAL FIELD OF INVENTION

The present invention relates to a novel manufacturing process for an integrated optical modulator based on graphene for the expressed purpose of data transfer characterized by [1] low cost and [2] enhanced manufacturing efficiency in the creation of [3] a high-performance high-efficiency optical modulator device by utilizing a [4] modified dry-transfer technique and [5] CVD-grown graphene that enables Graphene to be manufactured at low-cost while [6] maintaining compatibility with CMOS processing. The novel manufacturing process allows graphene based electronic devices to be mass-produced at low cost whilst maintaining high degrees of performance thereby facilitating the proliferation of ultra-broadband data transference base on optical technology. The present novel manufacturing process allows for the efficient and expedited-process commercialization of graphene based technology with respect to optical modulators.

BACKGROUND OF INVENTION

The field at present has witnessed the continuous advancement towards smaller, faster, and more efficient electronic devices for digital circuits that involve signal processing and communications. Today, state-of-the-art microprocessors use ultrafast transistors with geometric dimensions on the order of tens of nanometers. However, the miniaturization of these devices has also brought about new challenges. The thermal dissipation, signal delay, and power efficiency issues have created a substantial limitation to the speed of digital circuits. In recent years, it has become evident that bandwidth-limited electrical interconnect circuits can no longer meet the growing demand for data processing and telecommunications traffic. Besides the limited capacity, electrical circuits suffer from large energy consumption, signal attenuation and significant operational costs as interconnect densities rise. To address these challenging issues, the use of optical devices to replace electronic devices has attracted an increasing interest.

Optical devices enable huge amounts of data to be moved at very high speeds using extremely low power over very small optical waveguides. The use of optical devices has the potential of revolutionizing communications equipment because of the extremely large bandwidth, very low propagation loss, and an intrinsic lack of electromagnetic interference. Integration of electronics and photonics for future applications requires an efficient conversion of electrical signals to optical signals. One of the key

components of future telecommunications networks are optical modulators which serve as the gateway from the electrical to the optical domain. Optical modulators such as dielectric photonic devices can carry digital data with a huge capacity that is 1000 times greater than electronic devices, as a result of the high frequency of an optical electromagnetic wave. An optical modulator can modify the properties of light and are usually based on interference, resonance and bandgap absorption. However, optical modulators based on conventional materials (such as silicon, germanium and other compound semiconductors) suffer from slow switching times, narrow operating bandwidth and a large footprint. Therefore, there is a pressing need to develop new technologies which will enable enhanced operating conditions over a small active region for the development of optical modulators.

In general, an optical modulator is a device which can be used for manipulating a property of a light beam, e.g. a laser beam. Depending on which property of light is controlled, modulators are called intensity modulators, phase modulators, polarization modulators, spatial light modulators, etc. Presently most optical modulators for on-chip optical interconnects are usually based on electro-optical or electro-absorptive effects in materials such as silicon, germanium, and compound semiconductor hetero-structures. However, the device footprint of silicon-based modulators is typically larger than 100 μm2 due to its weak electro-optical properties. Germanium and compound semiconductors, on the other hand, face major challenges with integration with existing silicon electronics and photonics platforms. Integrating silicon modulators with high-quality-factor optical resonators increases the modulation strength, but these devices suffer from intrinsic narrow bandwidth and require sophisticated optical designs. Furthermore, they also have stringent fabrication requirements and limited temperature tolerances. Therefore, developing a complementary metal-oxide semiconductor (CMOS)-compatible material with adequate modulation speed and strength has become a task of not only scientific interest, but also industrial importance. Recently, as a candidate material for novel optical modulators, graphene has attracted a surge of interest in the academic world, because successful research work on broadband electro-absorption modulator based on inter-band absorption of graphene has been demonstrated by Liu et. al. in 2011.

Graphene is a promising material for realizing more advanced modulators due to its excellent electronic and optical properties. There are several distinctive advantages of graphene-based electro-absorption modulators: [1] Stronger light coupling or interaction with light compared conventional photonic semiconductors; [2] As the dynamic conductivity at high frequency for Dirac fermions is constant, the optical absorption of graphene is independent of wavelength, covering all telecommunications bandwidth and also the mid- and far-infrared; [3] With a carrier mobility exceeding 200,000 cm2V-1s-1 at room temperature , the Fermi level and hence the optical absorptions of graphene can be rapidly modulated through controlling the gate-variable optical conductivity depending on the carrier density and graphene quality; [4] The athermal optoelectronic properties of graphene and its CMOS-compatible integration processes at wafer scale make it a promising candidate for CMOS electronics, particularly for high frequency applications. Therefore, graphene can provide the highest saturable absorption for a given amount of material - a phenomenon which enables highly efficient electro-absorption modulators to be realized. The monolithic integration of a graphene electro-absorption modulator could open new routes to integrated photonic devices, with a compact footprint, low voltage operation and ultrafast modulation across a broad range of optical wavelengths.

Up to date despite many graphene-based optical modulators that have been fabricated in labs, which have demonstrated promising an application potential for modulation, they still face four major challenges

which hinder the development of this class of modulators for potential applications. The first challenge is related to the weak optical absorption of graphene in an entire device. Graphene has a high absorption coefficient, but it only absorbs 2.3% of normal incident light in suspended conditions because it has an atomic thickness which is too short for light-mass interaction. Therefore, research and development on optical field distribution or concentration in the device architecture, which exhibits high optical absorption efficiency, high speed and broad bandwidth, is quite necessary. The second challenge is related to design of the layouts of graphene and electrodes. For example, the existence of graphene will bring about capacitance effects which will prevent high frequency electrical signal input, which is much lower than the theoretical predicted frequency value. The third challenge is related to the modulation slope and depth. In current experimental devices, graphene layers are usually affected by the unwanted doping from substrates or metallic contacts, which influence the band structures and weaken the modulation capability. The fourth challenge is related to the form of graphene currently used, which are exfoliated graphene flakes. For the lab-model device demonstration, small mechanically exfoliated graphene flakes without a substrate are usually used to obtain high carrier mobility. Carrier mobility remains within the same order of magnitude at elevated temperatures because the scattering mechanism is mainly caused by electron or hole puddles within a two-dimensional graphene sheet. However, in reality, these kinds of graphene flakes cannot be used for integration with low-cost silicon technology.

In regards to the challenges in the development of this technology into a fully commercialized product that can be manufactured in a time and cost effective manner, the complexities carry over. Currently the field does not possess the capability to commercialize graphene based devices regardless of how complete any given device may be in design due to the nature of manufacturing and processing graphene itself. Graphene could not be readily integrated into existing devices due not only to the previously mentioned challenges. The present novel manufacturing process overcomes these issues through the invention of a novel manufacturing process that addresses the previously mentioned challenges. Therefore, based on the previously mentioned techniques, there is a pressing need, which is further addressed by the present invention.

PRIOR ART

The following is a tabulation of some prior art that presently appear relevant:

| **Patent Number** | **Kind Code** | **Issue/Publication Date** | **Patentee** |
|---|---|---|---|
| US 2014/0056551 | A1 | 2014-02-27* | Liu et al. |
| US 2013/0101247 | A1 | 2013-04-25* | Cho et al. |
| US 2014/0056551 | A1 | 2014-09-11* | Avouris et al. |
| US 2014/0105553 | A1 | 2014-04-17* | Kim et al. |
| US 2011/0186818 | A1 | 2011-08-04* | Bowers et al. |
| US 8735985 | B2 | 2014-05-37 | Bowers et al. |
| US 2014/0023321 | A1 | 2014-02-23* | Lu et al. |

**Denotes Publication Date*

In US Patent Publication No. 2014/0056551 A1, by Liu et al. entitled "GRAPHENE BASED OPTICAL MODULATOR," an integrated optical modulator device with high modulation speed, small footprint, and large optical bandwidth with embodiments comprising a broadband, high-speed, waveguide-integrated electro-absorption modulator based on monolayer graphene is disclosed.

In US Patent Publication No. 2013/0101247 A1, by Cho et al. entitled “OPTICAL MODULATOR INCLUDING GRAPHENE,” an optical modulator including graphene is disclosed, the optical modulator employing two graphene layers on a semiconductor layer flanking on either side an optical waveguide. The invention discloses a deeper modulation depth, smaller size and/or high operating speed in various embodiments.

In US Patent Publication No. 2014/0254981 A1, by Avouris et al. entitled “GRAPHENE PLASMONIC COMMUNICATION LINK,” a plasmonic device comprising a signal transfer link includes a first plasmonic coupler, a second plasmonic coupler and an insulator layer for the expressed purpose of high frequency signal transfer is disclosed.

In US Patent Publication No. 2014/0105553 A1, by Kim et al. entitled “GRAPHENE PHOTONIC DEVICE,” a graphene photonic device implementing an optical modulator by using a graphene layer with the capacity of implementing a polarization controller for the efficient induction of the property of an optical signal is disclosed, in other embodiments including an additional dielectric layer on top of the graphene layer.

In US Patent Publication No. 2011/0186818 A1, by Bowers et al. entitled “DOPED GRAPHENE ELECTRONIC MATERIALS,” an electronic device comprising a doped graphene substrate characterized by an n-type defined region individually chemically functionalized and a p-type defined region individually chemically functionalized is disclosed. A method for the formation of said electronic device on a graphene substrate is further disclosed.

In US Patent Publication No. 8735985 B2, by Bowers et al. entitled “DOPED GRAPHENE ELECTRONIC MATERIALS,” an electronic device comprising a doped graphene substrate characterized by an n-type defined region individually chemically functionalized and a p-type defined region individually chemically functionalized is disclosed.

In US Patent Publication No. 2014/0023321 A1, by Lu et al. entitled “ELECTRO-OPTICAL WAVEGUIDE APPARATUSES AND METHODS THEREOF,” an electro-optical waveguide apparatus including a graphene sheet comprising of opposing surfaces sandwiched in a waveguide structure in conjunction with a tuning device and the method for the construction of said device is disclosed.

DEFICIENCIES OF PRIOR ART

The above discussed prior art is deficient for various reasons.

US Patent Publication No. 2014/0056551 A1 is deficient in that it [1] does not disclose a novel manufacturing process [2] does not disclose a low-cost manufacturing process and [3] does not disclose a high-efficiency manufacturing process. It [4] does not disclose a device that can in further embodiments be easily commercialized and [5] embodies an experimental device that does not address a distinct need in the field for mass-manufacturing capabilities. It [6] does not address a relevant method that allows for the commercialization of graphene for electronic devices in other embodiment.

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be easily commercialized and [5] embodies an experimental device that does not address a distinct need in the field for mass-manufacturing capabilities. It [6] does not address a relevant method that allows for the commercialization of graphene for electronic devices in other embodiment. It further [7] fails to disclose a completely conceptualized device.

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SUMMARY OF INVENTION

The manufacturing process for the high speed, ultra-broadband and low cost integrated optical modulators based on graphene disclosed in this invention overcomes the disadvantages and deficiencies of the prior art by providing for the following advantages.

*(1) Novel dry-transfer technique*

The novel manufacturing process disclosed allows for the low-cost high-efficiency manufacturing of graphene enhanced electronic devices and fills a need in the field for the capacity to mass manufacture graphene based electronic components. The novel coating, attachment and heating process allows for an expedited and efficient construction process for the critical graphene components and may be applied to graphene construct components varying in size, in other embodiments being compatible with the construction of other electronic devices. This technique addresses a need in the field for the capacity of manufacturing graphene of sufficient dimensions, quality, and functional characteristics as to be capable of being employed in a commercialized application outside laboratory testing and development functionality.

(2) *CMOS compatibility*

The novel manufacturing process disclosed is compatible with the CMOS process and comprises the characteristics of possessing less power dissipation than standard logic families and other complex electrical devices of a similar nature whilst allowing for enhanced manufacturing utilizing existing technology with proven capabilities in the field. This allows for ease of adoption, implementation and manufacturing due to low turn-around time because the fabrication, designing, testing, and implementing of custom machinery as well as the associated logistics are thus rendered unnecessary. The present novel manufacturing process allows for the creation of high-capability commercially viable graphene based optical modulators utilizing existing factory assembly techniques.

(3) *Utilizes existing manufacturing process*

Whereas the principle manufacturing technique disclosed demonstrates numerous novel advancements upon the field with regards to advancements made by the present invention, the principle manufacturing process in being CMOS compatible allows for the present invention to be actively and rapidly employed using existing CMOS techniques and technology. In utilizing well tested and adopted technology with proven capacity of creating advanced electronic component, it allows for the device as disclosed in the

present invention to be manufactured on a commercial scale at a comparable level of quality while maintaining relatively low cost and requiring no large-scale retooling and associated logistics.

(4) *Variable scale graphene layer fabrication capacity*

The present need in the field is represented by the inability to fabricate graphene layers of variable scale dependent on the application in a manner that aligns with current manufacturing and commercial standards. The present invention overcomes this deficiency and provides a solution to this need by the field by providing the ability to directly fabricate graphene layer components onto any select electronic device through the disclosed novel dry-transfer technique and CMOS compatibility thereby providing the field with the capacity of fabricating component integrated graphene layers to specification in a manner suitable for large scale low-cost manufacturing with an added time and logistics advantage.

(5) *Minimal turn-around commercial manufacturing compatibility*

The novel manufacturing process disclosed confers the advantage of allowing for minimal turn-around manufacturing compatible with current manufacturing technology. This allows the novel graphene based optical modulator device to be readily manufactured on existing assembly techniques the novel technique disclosed allows for current manufacturing devices the capacity to mass produce and integrate graphene layers into electronic devices with no conversion or adaptation and in other embodiments requiring minimal conversion or adaptation as dictated by design specifications.

DRAWINGS

FIG. 1 shows an illustration of the working principle of the disclosed graphene base optical modulator

FIG. 2 shows an illustration of the working principle of the proposed novel manufacturing process

DETAILED DESCRIPTION

In FIG. 1 **10**, an illustration of the working principle of the disclosed graphene optical modulators, based on a **11** basic silicon bus waveguide configuration as disclosed in the manufacturing process is shown. As shown in FIG. 1 the device structure is based on **12** double layer graphene. The silicon waveguide and **13** gold plasmonic structures are combined in order to integrate suspended graphene layers between them. The thickness of the **14** middle gold nanostripe is ~30 nm, and is optimized in the range of 20 nm - 100 nm in one embodiment. The width of the middle gold stripe is ~100 nm, and may be optimized in the range of 50 nm - 300 nm for the device in other embodiments. The middle gold strip is used for enhanced optical absorption efficiency of graphene. The configuration of the left and the right parallel gold electrodes allows for optimized drive voltage control. The thickness of the electrodes is ~50 nm. The **15** hBN layer with a thickness of ~2 nm is capped on the silicon bus waveguide and the top layer of graphene to electrically isolate graphene and the silicon waveguide, and to further isolate graphene and the middle gold stripe. The hBN layer is used instead of **16** SiO2 capping layer in order to avoid charge traps and to maintain high carrier mobility of graphene, and to also prevent the doping from Si and gold to graphene. The lengths of the silicon waveguide port sides are ~600 nm and 300 nm, respectively. Under the silicon waveguide, there is a SiO2 buried oxide layer of 2 µm. The length of the waveguide is L, which determines the light absorption efficiency of graphene. L is optimized across the range of 5 µm - 25µm as in the course of operation, the incident light is fed from one end of the

waveguide and collected from the other end. The disclosed dimensions can be further optimized and altered in other embodiments of the disclosed device as dictated by any alterations to specifications, design, intended purpose and or manufacturing process.

In FIG. 2 **17**, an illustration of the working principle of the fabrication process of graphene-based modulators involving three major steps based on a clean room process: (Step 1) preparation of a silicon-on-insulator (SOI) wafer with Si waveguides and buried oxide, (Step 2) deposition and structuring of graphene, and (Step 3) metallization is shown. The detailed description these steps are described as below. The processing is started using a **18** customized SOI wafer with integrated Si waveguides and buried oxide, purchased from commercial CMOS R&D vendors in one embodiment. The wafer is covered using plasma enhanced CVD with a 2-nm-thick layer of hBN to prevent electrical contact between the **19** graphene and the silicon waveguide. Upon completion of the disclosed procedure (Step 1), deposition and structuring of graphene (Step 2) is conducted. The graphene is high quality graphene on **20** copper foils for the device development is commercially sourced. As show in FIG. 2, Graphene is located on the SOI wafer using the disclosed dry transfer method. First, **21** Polymethylmethacrylate (PMMA) powder is dissolved in chlorobenzene. Then, PMMA solution (120 mg/mL) is spin-coated on a **22** graphene/copper foil at 2000 rpm for 30 s and dried in air. The **23** Polydimethylsiloxane (PDMS) block with a ~1 cm diameter hole is then be gently pressed down onto the PMMA/graphene/copper substrate. Next, the copper is etched with **24** ammonium persulfate (0.1 mol/L) and dried in air after rinsing it with distilled water. After that, the **25** PDMS/PMMA/graphene composite is placed on the target substrate having patterned silicon waveguides and heated at 160 oC for over 6 hr. The PDMS block is peeled off while the PDMS/PMMA/graphene composite is hot. Next, the PMMA/graphene on substrate is annealed in a furnace with Ar (~500 sccm) and H2 (~500 sccm) at 350 oC for about 3 hr to remove the PMMA. The resultant graphene sheet is etched in shape using oxygen plasma in areas of the disclosed device where this step is critical to the fabrication, construction and manufacturing process per disclosed design of applicable device. Once the above step of deposition and structuring of graphene (Step 2) is completed, the fabrication process enters enter into the step of metallization for the contact electrodes (Step 3). The contact electrodes are fabricated using electron-beam lithography and metal deposition. The metal deposition uses the following two steps. In the first step, a nominally 1-nm-thick Ti layer is evaporated, followed by a 20-nm-thick Au layer. The Ti serves to improve the adhesion of silver to graphene and does not form a continuous layer. In the second step, a 25-nm-thick Au layer is sputtered to ensure that the waveguide sidewalls are covered with metal to achieve electrical contact between the central electrode and the bonding pad. Keeping the Ti content as low as possible is crucial, as its dissipative dielectric function leads to a strong damping of the optical mode. The device is annealed in vacuum at 125 °C for several hours to remove PMMA residues from the surface of the graphene. Finally, the device is cleaved using a diamond scribe to obtain a clean facet for the in-coupling of light.

CLAIMS

What is claimed is:

1. A method for the manufacturing process for a graphene based device comprising:

(a) A first step preparing of the SOI wafer;
(b) A second step depositing and structuring the graphene;
(c) A third step completing metallization.

2. The method as set forth in claim **1**, wherein said preparation the SOI wafer comprises Si waveguides and buried oxide.

3. The method as set forth in claim **1**, wherein said preparation the SOI wafer comprises buried oxide.

4. The method as set forth in claim **1**, wherein said wafer is covered using plasma enhanced CVD.

5. The method as set forth in claim **1**, wherein said wafer is with a layer of hBN.

6. The method as set forth in claim **5**, wherein said layer of hBN is 2-nm-thick layer.

7. The method as set forth in claim **5**, wherein said hBN to prevent electrical contact between the graphene and the silicon waveguide.

8. The method as set forth in claim **1**, wherein said graphene is a high quality graphene on copper foil film.

9. The method as set forth in claim **8**, wherein said graphene on copper foil film contains PMMA solution (120 mg/mL) is spin-coated onto it.

10. The method as set forth in claim **9**, wherein said PMMA solution is120 mg/mL.

11. The method as set forth in claim **9**, wherein said PMMA solution is comprised of PMMA powder.

12. The method as set forth in claim **11**, wherein said PMMA powder is dissolved in chlorobenzene.

13. The method as set forth in claim **9**, wherein said spin-coating is performed at 2000 rpm.

14. The method as set forth in claim **9**, wherein said spin-coating is performed for 30 seconds.

15. The method as set forth in claim **9**, wherein said spin-coating is dried in air.

16. The method as set forth in claim **9**, wherein said PMMA forms a PDMS/PMMA/graphene/copper substrate.

17. The method as set forth in claim **9**, wherein said PDMS forms PDMS blocks.

18. The method as set forth in claim **9**, wherein said PDMS blocks are pressed onto the PMMA/graphene/copper substrate.

19. The method as set forth in claim **9**, wherein said PDMS/PMMA/graphene composite is placed on the target substrate.

20. The method as set forth in claim **19**, wherein said target substrate contains patterned silicon waveguides.

21. The method as set forth in claim **20**, wherein said target substrate is heated at 160 degrees Celsius.

22. The method as set forth in claim **21**, wherein said target substrate is heated for a minimum of 6 hours.

23. The method as set forth in claim **18**, wherein said PDMS blocks are peeled off while the PDMS/PMMA/graphene composite is hot.

24. The method as set forth in claim **23**, wherein said composite forms a PMMA/graphene on substrate.

25. The method as set forth in claim **24**, wherein said PMMA/graphene on substrate annealed in a furnace with Ar (~500 sccm).

26. The method as set forth in claim **24**, wherein said PMMA/graphene on substrate annealed in a furnace with and H2 (~500 sccm).

27. The method as set forth in claim **24**, wherein said PMMA/graphene on substrate annealed in a furnace at 350 degrees Celsius.

28. The method as set forth in claim **24**, wherein said PMMA/graphene on substrate annealed in a furnace for 3 hours.

29. The method as set forth in claim **24**, wherein said PMMA/graphene on substrate annealed in a furnace to remove the PMMA.

30. The method as set forth in claim **24**, wherein said PMMA/graphene on substrate results in the formation of a graphene sheet is etched in shape using oxygen plasma.

31. The method as set forth in claim **30**, wherein said etching is conducted using oxygen plasma.

32. The method as set forth in claim **1**, wherein said metallization creates the contact electrodes.

33. The method as set forth in claim **32**, wherein said electrodes are fabricated using electron-beam lithography and metal deposition.

34. The method as set forth in claim **32**, wherein said electrodes are fabricated using deposition.

35. The method as set forth in claim **32**, wherein said metallization occurs in two stages.

36. The method as set forth in claim **35**, wherein said stages comprises a first step in which a nominally 1-nm-thick Ti layer is evaporated.

37. The method as set forth in claim **35**, wherein said stages comprises a first step in which a 20-nm-thick Au layer is evaporated.

38. The method as set forth in claim **35**, wherein said stages comprises a second step in which a 25-nm-thick Au layer is sputtered.

39. The method as set forth in claim **38**, wherein said Au layer is sputtered to ensure that the waveguide sidewalls are covered with metal.

40. The method as set forth in claim **35**, wherein said metal ensures electrical contact between the central electrode and the bonding pad.

41. The method as set forth in claim **36**, wherein said Ti serves to improve the adhesion of silver to graphene and does not form a continuous layer.

42. The method as set forth in claim **36**, wherein said Ti does not form a continuous layer.

43. The method as set forth in claim **1**, wherein said device is annealed in vacuum at 125 °C.

44. The method as set forth in claim **43**, wherein said device is annealed to remove PMMA residues from the surface of the graphene.

45. The method as set forth in claim **43**, wherein said device is cleaved using a diamond scribe to obtain a clean facet for the in-coupling of light.

46. The device as set forth in claim **1**, wherein said graphene based device is an optical modulator device.

47. The device as set forth in claim **46**, wherein said graphene based device is a high speed device.

48. The device as set forth in claim **46**, wherein said graphene based device is a ultra-broadband device.

49. The device as set forth in claim **46**, wherein said graphene based device is an integrated optical modulator device.

50. The device as set forth in claim **46**, wherein said graphene optical modulator comprises a silicon bus waveguide.

51. The device as set forth in claim **46**, wherein said graphene optical modulator comprises double layers of graphene.

52. The device as set forth in claim **46**, wherein said graphene optical modulator comprises two gold plasmonic structures.

53. The device as set forth in claim **52**, wherein said plasmonic structures are in parallel configuration.

54. The device as set forth in claim **52**, wherein said plasmonic structures combine to integrate suspended graphene layers between them.

55. The device as set forth in claim **46**, wherein said graphene optical modulator comprises a middle gold nanostripe.

56. The device as set forth in claim **55**, wherein said gold nanostripe is optimized in the range of 20 nm to 100 nm range in one embodiment.

57. The device as set forth in claim **55**, wherein said gold nanostripe is optimized at the range of 50 nm to 300 nm range in one embodiment.

58. The device as set forth in claim **55**, wherein said gold nanostripe is used for enhanced optical absorption efficiency of graphene.

59. The device as set forth in claim **52**, wherein said gold plasmonic structures are electrodes.

60. The device as set forth in claim **59**, wherein said electrodes allow for optimized drive voltage control.

61. The device as set forth in claim **59**, wherein said electrodes are 50 nm.

62. The device as set forth in claim **46**, wherein said graphene optical modulator comprises an hBN layer.

63. The device as set forth in claim **62**, wherein said hBN layer is 2 nm.

64. The device as set forth in claim **62**, wherein said hBN layer is capped on the silicon bus waveguide.

65. The device as set forth in claim **62**, wherein said hBN layer functions to electrically isolate the graphene and the silicon waveguide.

66. The device as set forth in claim **62**, wherein said hBN layer functions to isolate the graphene and the middle gold stripe.

67. The device as set forth in claim **62**, wherein said hBN layer maintains high carrier mobility of graphene.

68. The device as set forth in claim **62**, wherein said hBN layer prevents the doping of Si and gold to the graphene.

69. The device as set forth in claim **50**, wherein said silicone waveguide comprises side ports.

70. The device as set forth in claim **69**, wherein said side port is 600 nm.

71. The device as set forth in claim **69**, wherein said side port is 300 nm.

72. The device as set forth in claim **50**, wherein said silicone waveguide buries aSiO2 oxide layer.

73. The device as set forth in claim **72**, wherein said SiO2 oxide layer is 2 μm.

74. The device as set forth in claim **50**, wherein said silicone waveguide determines the light absorption efficiency of graphene.

75. The device as set forth in claim **50**, wherein said silicone waveguide is optimized across the range of 5μm - 25μm.

76. The device as set forth in claim **74**, wherein said light is incident light.

77. The device as set forth in claim **76**, wherein said incident light is fed from one end of the waveguide.

78. The device as set forth in claim **76**, wherein said incident light is collected at the other end of the waveguide.

ABSTRACT

A novel manufacturing process for an integrated optical modulator based on graphene for the expressed purpose of data transfer characterized by low cost and enhanced manufacturing efficiency in the creation of a high-performance high-efficiency optical modulator device by utilizing a modified dry-

transfer technique and CVD-grown graphene that enables Graphene to be manufactured at low-cost while maintaining compatibility with CMOS processing is disclosed.

REFERENCE NUMERALS

| | |
|---|---|
| 10 | Illustration of the working principle of the disclosed graphene base optical modulator |
| 11 | Silicon bus waveguide |
| 12 | Double layer graphene |
| 13 | Gold plasmonic structures |
| 14 | Middle gold nanostripe |
| 15 | hBN layer |
| 16 | SiO2 capping layer |
| 17 | Illustration of the working principle of the proposed novel manufacturing process |
| 18 | SOI wafer |
| 19 | Graphene |
| 20 | Copper foils |
| 21 | Polymethylmethacrylate |
| 22 | Graphene/copper foil |
| 23 | Polydimethylsiloxane |
| 24 | Ammonium persulfate |
| 25 | PDMS/PMMA/graphene composite |

# DRAWINGS

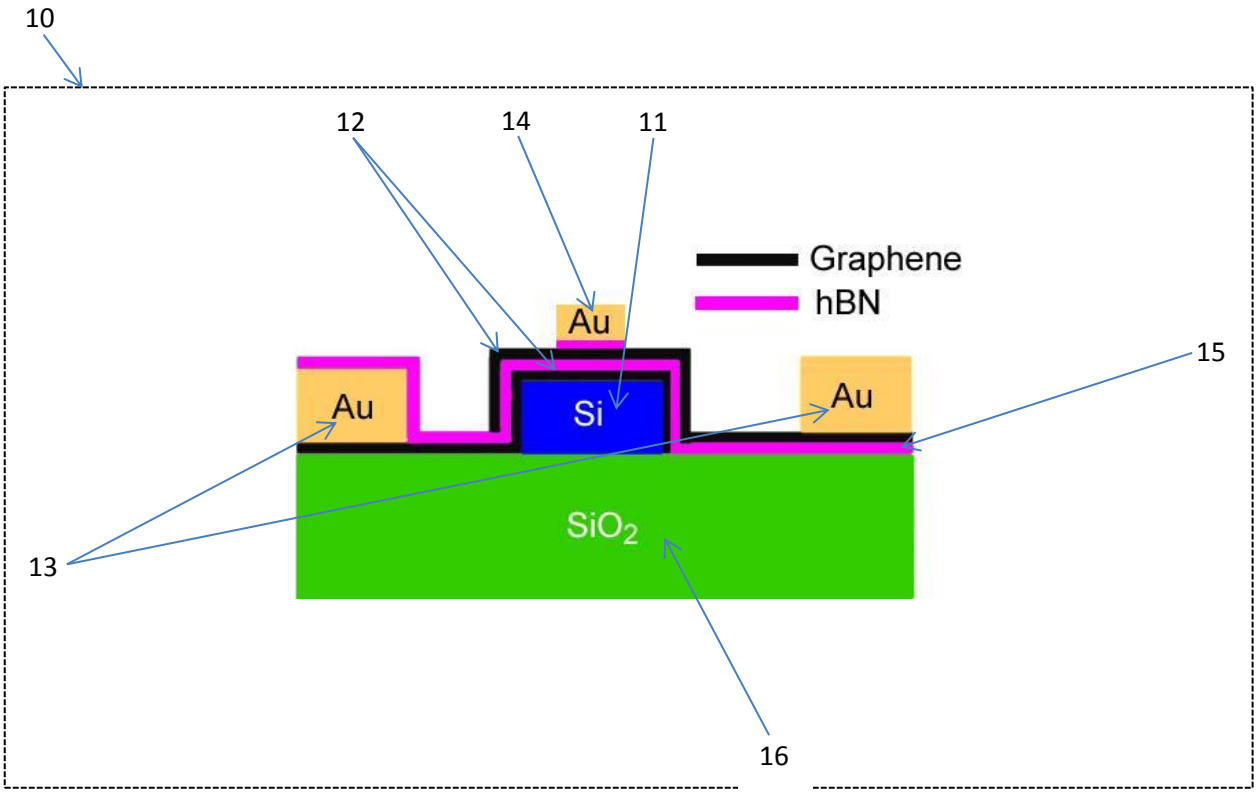


**FIGURE 1**

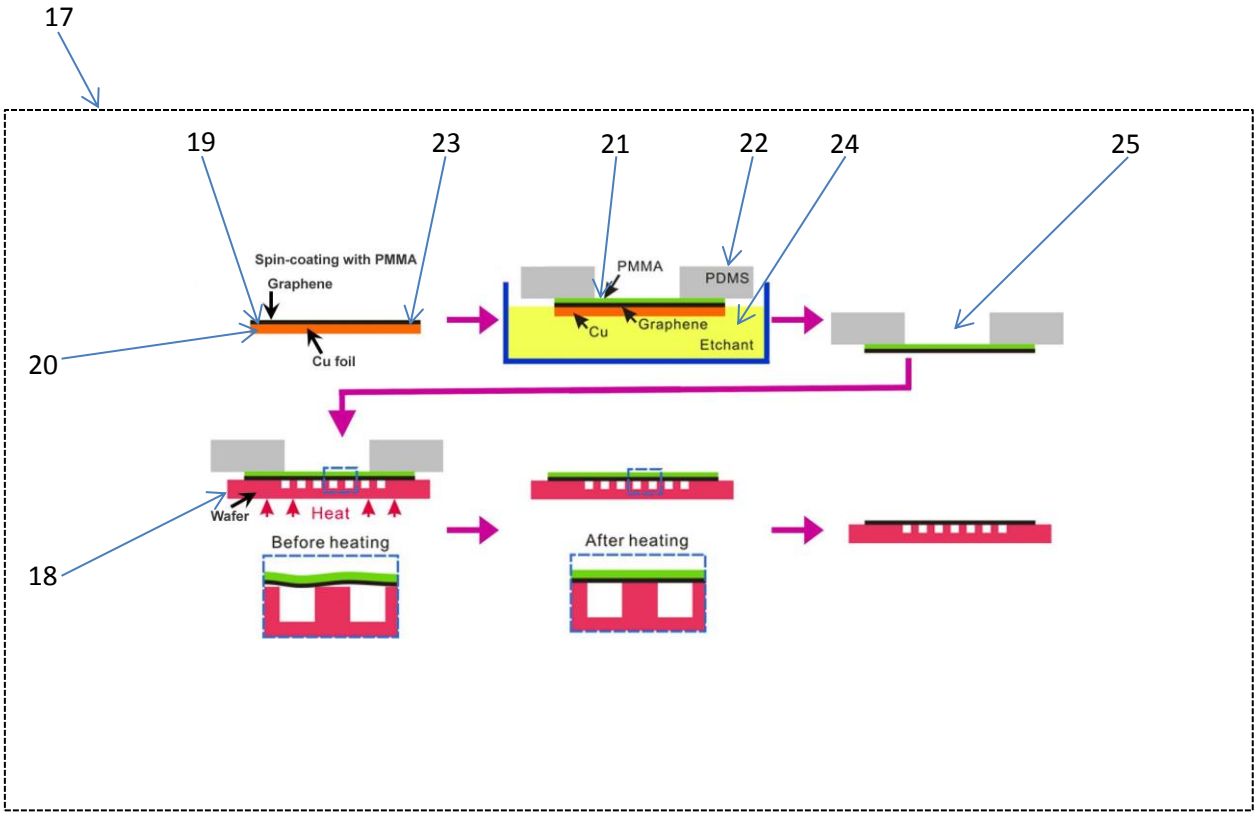
17
19
23
21
22
24
25
Spin-coating with PMMA
Graphene
Cu foil
20
PMMA
PDMS
Cu
Graphene
Etchant
Wafer
Heat
Before heating
After heating
18

**FIGURE 2**